REMARKS/ARGUMENTS

STATUS OF THE APPLICATION

After entry of this amendment, claims 20, 23, 25-28 and 30-36 will be pending in this application. Claim 36 has been added. Claims 23, 25-28,and 30-35 have been amended.

Support for the new and amended claims can be found in the specification, no new matter has been added. In particular, support for an array processor comprising at least two arithmetic processing units (i.e., two of APU 970) can be found at least on page 21, lines 26-33, and Figure 3 of the specification. Support that an APU 970 can include three MAC units 900 can be found at least on page 19, lines 5-6, and Figure 2 of the specification.

Claim 20 was allowed.

Claims 23, 25-28, and 30-35 were rejected under 35 U.S.C. 102(b) as being anticipated by Yamauchi et al., "Architecture and Implementation of a Highly Parallel Single-Chip Video DSP" ("Yamauchi").

Reconsideration and allowance of the pending claims is respectfully requested in light of these amendments and remarks.

THE CLAIMS

Claims 23-26

Applicants respectfully submit that Yamauchi does not teach or suggest each and every feature recited in claim 23. For example, claim 23 recites, in part, "... the first array processor comprises at least two arithmetic processing units, each of the at least two arithmetic processing units comprises: ... a shared operand unit coupled to provide a shared operand to the first MAC unit, the second MAC unit, and the third MAC unit; and ... ." Nowhere does Yamauchi teach or suggest an array processing unit as recited in claim 23.

For example, Examiner cites WM or IN1 of Yamauchi's Figure 2 as being a shared operand unit of claim 23. (See Office Action: p. 2). However, with respect to IN1, this structure only couples to two DPUs, which Examiner analogizes as MAC units. Accordingly, IN1 is not a shared operand unit coupled to provide a shared operand to the first MAC unit, the

second MAC unit, and the third MAC unit. With respect to WM, nowhere does Yamauchi teach or suggest that an array processor have at least two shared operand units. Figure 2 of Yamauchi discloses only one WM for the IDSP function block.

Therefore, for at least these reasons, claim 23 should be allowed.

Claims 24-26, which depend from claim 23, should at least be allowed for a similar rationale as discussed for claim 23.

Claims 27-30

Applicants respectfully submit that Yamauchi does not teach or suggest each and every feature recited in claim 27. For example, claim 27 recites, in part, "... array processor comprising: ... a first shared output and feedback circuit configured to receive data from the first MAC unit, the second MAC unit, and third MAC unit, and further configured to provide data to the first local memory, the second local memory, and the third local memory; ... and a second shared output and feedback circuit configured to receive data from the fourth MAC unit and the fifth MAC unit, and further configured to provide data to the fourth local memory and the fifth local memory."

Accordingly, claim 27 should be allowed for at least these reasons.

Claims 28-30, which depend from claim 27, should be allowed for at least a similar rationale as discussed for claim 27.

Claims 31-36

Claim 31 recites, in part, "... array processor comprises: ... a first shared operand unit coupled to the first MAC unit, the second MAC unit, and the third MAC unit, and a second shared operand unit coupled to the fourth MAC unit, the fifth MAC unit, and the sixth MAC unit." As discussed above, Yamauchi fails to teach or suggest these features.

Accordingly, claim 31 should be allowed for at least these reasons.

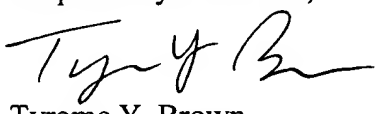
Claims 32-36, which depend from claim 31, should be allowed for at least a similar rationale as discussed for claim 31.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this application are in condition for allowance. The issuance of a notice of allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-752-2456.

Respectfully submitted,



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Attachments
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